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EXAMINER	
TRIMMINGS, JOHN P	
ART UNIT	**PAPER NUMBER**
2133	5

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/976,523	DORSEY, MICHAEL C.	
	Examiner	Art Unit	
	John P Trimmings	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 October 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32* is/are rejected.

7)☒ Claim(s) *1,2,8,10,11,18,* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 October 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-32 are presented for examination.

Information Disclosure Statement

The examiner has considered the applicant's Disclosure Statements of 3/27/2003.

Drawings

1. The drawings are objected to because:

   a. FIG.2 LSSD and STEP CLKS are not referred to in the disclosure.

   b. FIG.9 LSSD_CLKA, LSSD_CLKB, LBST_SCAN_CLKA and LBST_SDCAN_CLKB are not referred to in the disclosure.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

2. The disclosure is objected to because of the following informalities:

   a. Page 5 line 21 recites "synchronous random access memory ("SRAMs")". The statement is a combination of two terms; "Static Random Access Memory, an SRAM", and "Synchronous Dynamic Random Access Memory, an SDRAM", the terms of which are generally accepted in the

art. The examiner suspects that the applicant wishes to recite; "static random access memory", but would like the applicant to respond as to the device type specifically intended. Appropriate correction is required.

b. The disclosure is objected to because of the following informalities: page 7 line 6 describes engine 110 being configured by a 66 bit signal composed of a 32 bit vector and 33 bit seed. The sum of 32 and 33 is not 66. Appropriate correction is required.

c. The disclosure is objected to because of the following informalities: page 10 line 1 recites, "LBST_STEP_STEPE", but the examiner cannot find this reference in FIG.9. Appropriate correction is required.

d. The disclosure is objected to because of the following informalities: page 10 line 9 recites, "components 150", but the examiner cannot find this reference in the drawings. Appropriate correction is required.

e. The disclosure is objected to because of the following informalities: page 11 line 19 and 22, page 13 line 33 recite, "ASIC 100", but the examiner cannot find this reference in the drawings, and believes it should read "ASIC 150". Appropriate correction is required.

f. The disclosure is objected to because of the following informalities: page 12 line 32 recites, "initialized them to...", but the examiner believes it should read "initialized to...". Appropriate correction is required.

Claim Objections

3. Claims 1, 2, 8, 10, 11 and 18 are objected to because of the following informalities: the claims each contain the phrase "capable of", which is not a positive limitation. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 5 recites the limitation "the logic built-in self-test signature" and "the stored results". There is insufficient antecedent basis for these limitations in the claim.

5. Claim 14 recites the limitation "the logic built-in self-test signature" and "the stored results". There is insufficient antecedent basis for these limitations in the claim.

6. Claim 19 recites the limitation "the built-in self-test controller". There is insufficient antecedent basis for this limitation in the claim.

7. Claim 21 recites the limitation "the performed built-in self-test ". There is insufficient antecedent basis for this limitation in the claim.

8. Claim 23 recites the limitation "the dual mode built-in self-test controller". There is insufficient antecedent basis for this limitation in the claim.

9. Claim 24 recites the limitation "the multiple input signature register" (two times) and "the stored results". There is insufficient antecedent basis for these limitations in the claim.

10. Claim 25 recites the limitation "the performed built-in self-test. There is insufficient antecedent basis for this limitation in the claim.

11. Claim 26 recites the limitation "the results of the performed built-in self-test". There is insufficient antecedent basis for this limitation in the claim.

12. Claim 28 recites the limitation "the dual mode built-in self-test controller". There is insufficient antecedent basis for this limitation in the claim.

13. Claim 29 recites the limitation "the multiple input signature register" (two times), and "the stored results". There is insufficient antecedent basis for these limitations in the claim.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

14. Claims 1, 2, 6-10, 15, 17and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Motika et al., U.S. Patent No. 5982189, and in view of Rosno et al., U.S. Patent No. 6535986.

As per Claims 1 and 7:

Motika et al. teaches a built-in self-test controller (FIG.2 50) and means, comprising a logic built-in self-test domain (FIG.2 34, 38) being capable of performing a logic built-in self-test (column 3 lines 6-66). However, Motika et al. fails to specify the test circuit testing at a test frequency at least as slow as a slowest frequency of a plurality of timing domains to undergo the logic built-in self-test. But in an analogous art, Rosno et al. does teach this feature in columns 1 lines 64-67 and column 2 lines 1-12, and also column 3 lines 66-67 and column 4 lines 1-10. It would have been obvious to one with ordinary skill to add the features of Rosno et al. to Motika et al. in order to run the circuits at frequencies low enough to pass test. And Rosno et al., in column 2 lines 63-67 explains the need to have the capability to adjust the clock frequencies of circuits under test. And one with ordinary skill in the art at the time of the invention, motivated as suggested in Rosno et al., would combine the references and so the claims are rejected.

As per Claims 2 and 8:

Motika et al. further teaches the built-in self-test controller and means of claims 1 and 7, wherein the logic built-in self-test domain comprises: a logic built-in self-test state machine (FIG.2 34), and a pattern generator capable of generating a scan pattern for use in a state of the logic built-in self-test state machine (column 3 lines 56-67 and column 4 lines 1-5). And in view of the motivation previously mentioned in Claims 1 and 7 above, the claims are rejected.

As per Claims 6, 9, 15 and 19:

Motika et al. further teaches the built-in self-test controller and means of claims 1, 7, 10 and 17, further comprising a memory built-in self-test domain (FIG.2 32, 36). And in view of the motivation mentioned in Claims 1, 7, 10 and 17, the claims are rejected.

As per Claims 10 and 17:

Motika et al. teaches an integrated circuit device, comprising: a plurality of memory components (FIG.2 36); a logic core (FIG.2 38); a testing interface (FIG.2 60); and a built-in self-test controller controlled through the testing interface (FIG.2 50), comprising a logic built-in self-test domain (FIG.2 34, 38) capable of performing a logic built-in self-test (column 3 lines 64-66). But Motika et al. fails to teach the circuit testing at a test frequency at least as slow as a slowest frequency of a plurality of timing domains to undergo the logic built-in self-test. But in an analogous art, Rosno et al. does teach this feature in columns 1 lines 64-67 and column 2 lines 1-12, and also column 3 lines 66-67 and column 4 lines 1-10. It would have been obvious to one with ordinary skill to add the features of Rosno et al. to Motika et al. in order to run the circuits at frequencies low enough to pass test. And Rosno et al., in column 2 lines 63-67 explains the need to have the capability to adjust the clock frequencies of circuits under test. One with ordinary skill in the art at the time of the invention, motivated as suggested in Rosno et al., would combine the references and so the claims are rejected.

15. Claims 11 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Motika et al., U.S. Patent No. 5982189, and in view of Rosno et al., U.S. Patent

No. 6535986 as applied to Claims 1, 7 and 10 above, and further in view and in view of Koproski et al., U.S. Patent No. 6671838. The subject claims limit the LBIST to comprise an LBIST state machine and pattern generator, and the Motika et al. and Rosno et al. references fail to teach this limitation. In an analogous art, Koproski et al., in column 3 lines 1-5 teaches a state machine for an LBIST device, and, in FIG.1, Koproski et al. teaches a pattern generator 4. It would have been obvious to one with ordinary skill to utilize a state machine to control a pattern generator as taught by Koproski et al. in the subject circuit. And in column 1 lines 1-67 and column 2 lines 1-28, the reference states the advantage of using a special analysis system for creating weighted patterns for testing in an LBIST. One with ordinary skill in the art at the time of the invention, motivated by Koproski et al., would combine the references, and so the claims are rejected.

16. Claims 3 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Motika et al., U.S. Patent No. 5982189, in view of Rosno et al., U.S. Patent No. 6535986 as applied to Claims 2 and 11, and further in view of Zuraski et al., U.S. Patent No. 6560740, Lo et al., U.S. Patent No. 5661732, and Wong et al., U.S. Patent No. 6636997. The LBIST state machine in Claims 2 and 11 above is further limited to a reset state entered via an external signal. Zuraski et al. enters a state via an external reset signal (Zuraski et al, column 10 lines 31-36), an obvious modification in order to control the test circuit during test, but does not begin initializing the device with an LBIST run signal. In an analogous art, Lo et al., enters a 1st state subsequent to a start ABIST signal (Lo et al. column 5 lines 6-8), and suggests a similar LBIST on the same

chip (column 6 lines 9-12). In order to control operation of the test cycles, it would have been obvious to provide the features of Lo et al. in the same circuit under consideration. And finally, Wong et al. in column 6 lines 26-50 teaches the states of scan, step, and complete (done) as specified by the applicant's claim. One with ordinary skill would have found it obvious to apply the steps of Wong et al. to the state machine of Lo et al. in performance of an LBIST test. Wong et al., in column 2 lines 62-67, describes an advantage of the invention as being capable of both pseudo-random and functional testing. Lo et al. column 2 lines 38-40 lists an advantage of the invention as being an improvement in test time and test coverage. And Zuraski Jr. et al., professes the advantages (column 2 lines 10-18) of a readily programmable BIST that would not need constant revision as needs change. In view of the motivations for Zuraski et al. and Lo et al., and in view of Wong et al., one with ordinary skill in the art at the time of the invention, would combine all of the references above, thus the claims are rejected.

17. Claims 4 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Motika et al., U.S. Patent No. 5982189, in view of Rosno et al., U.S. Patent No. 6535986 as applied to Claims 2 and 11, and further in view of Rajski et al., U.S. Patent No. 6684358. The controller of Claims 2 and 11 is limited wherein the pattern generator is an LFSR seeded with a primitive polynomial. In an analogous art, Rajski et al., in column 8 lines 6-9 teaches such pattern generator. It would have been obvious to one with ordinary skill to modify the system in question to include a highly reliable primitive polynomial to the LFSR in order to get better test coverage. In column 2 lines 15-33, Rajski et al. recites the advantage of this improved pattern generator that allows fuller

test coverage than predecessors. And one with ordinary skill in the art at the time of the invention, motivated as suggested by Rajski et al., would combine the references, and so the claims are rejected.

18. Claims 5 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Motika et al., U.S. Patent No. 5982189, in view of in view of Rosno et al., U.S. Patent No. 6535986 as applied to Claims 2 and 11, in view of Hong-Shin Jun, U.S. Patent No. 6658611, and further in view of Au et al., U.S. Patent No. 6681359. The controller of Claims 2 and 11 is limited wherein the signature includes an error bit (Jun column 5 lines 43-63) and a "done" bit (Au et al. column 9 lines 25-33). It would have been obvious to apply the teachings therefrom in order to facilitate control of test states. Jun cites an improved programmable BIST using optimum test patterns (column 2 lines 10-13), and Au et al. cites control of BIST using a standard interface (column 2 lines 18-26). And one with ordinary skill in the art at the time of the invention, motivated as suggested above would combine the references, and therefore the claims are rejected.

19. Claims 16 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Motika et al., U.S. Patent No. 5982189, and in view of Rosno et al., U.S. Patent No. 6535986 as applied to Claims 10 and 17, and further in view of Au et al., U.S. Patent No. 6681359. The integrated circuit device of claims 10and 17 is limited wherein testing interface comprises a Joint Test Action Group tap controller. Au et al., in the Abstract teaches this feature, and cites the advantage of a controller of BIST circuits using a standard JTAG interface (column 2 lines 18-26) as being applicable to more effective test control. It would have been obvious to apply the teachings of Au et al. and

to provide a standard interface for test purposes. And one with ordinary skill in the art at the time of the invention, motivated as suggested above, would combine the references, and therefore the claim is rejected.

20. Claims 21 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rosno et al., U.S. Patent No. 6535986, in view of Kraus et al., U.S. Patent No. 6587979. Rosno et al. teaches a method for performing a BIST (see Abstract) on an IC device, and test circuit for testing at a test frequency at least as slow as a slowest frequency of a plurality of timing domains to undergo the logic built-in self-test. Rosno et al. teaches this feature in columns 1 lines 64-67 and column 2 lines 1-12, and also column 3 lines 66-67 and column 4 lines 1-10. But not specified is that the controller be reset externally. However, in an analogous art, the BIST of Kraus et al., resets the BIST controller of FIG.7 by way of the tester 21 (column 9 lines 52-58), and performs a BIST (column 15 lines 24-35), and obtains results (column 8 lines 10-36) of the BIST. It would have been obvious to provide a means of resetting the circuit under test as taught by Kraus et al. to improve test flexibility. And column 2 lines 32-40 of Kraus et al. explains the attributes of the invention as being a highly adaptable and flexible platform for testing, and one with ordinary skill in the art at the time of the invention, motivated by Kraus et al., would combine the references, as so the claims are rejected.

21. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Rosno et al., U.S. Patent No. 6535986, in view of Kraus et al., U.S. Patent No. 6587979 as applied to Claim 21, and further in view of Rajski et al., U.S. Patent No. 6684358. Rosno et al. and Kraus et al. fail to further teach the claim limits of resetting a MISR and a

pattern generator in an LBIST. Rajski et al. performs these functions on an LBIST (column 4 lines 10-57). And it would have been obvious to apply this reset to the control circuits prior to start-up of the subject test thereby guaranteeing a starting basis. In column 2 lines 15-33, Rajski et al. recites an improved pattern generator that allows fuller test coverage than predecessors. One with ordinary skill in the art at the time of the invention, motivated as suggested by Rajski et al., would combine the references, and so the claim is rejected.

22. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Rosno et al., U.S. Patent No. 6535986, in view of Kraus et al., U.S. Patent No. 6587979 as applied to Claim 21, and further in view of Zuraski et al., U.S. Patent No. 6560740, Lo et al., U.S. Patent No. 5661732, and Wong et al., U.S. Patent No. 6636997. Rosno et al. and Kraus et al. fail to further teach the BIST state machine in Claim 21 as further limited to a reset state entered via an external signal. However, Zuraski et al. enters a state via an external reset signal (Zuraski et al, column 10 lines 31-36), which would have been obvious to apply in order to initialize a test circuit. But Zuraski et al. does not begin initializing the device with an LBIST run signal. In an analogous art, Lo et al., enters a 1st state subsequent to a start ABIST signal (Lo et al. column 5 lines 6-8), and suggests a similar LBIST on the same chip (column 6 lines 9-12). It would have been obvious to apply the teachings of Zuraski et al. and Lo et al. in order to begin testing with a reset sequence of the circuit under test. And finally, Wong et al. in column 6 lines 26-50 teaches the states of scan, step, and complete (done) as specified by the applicant's claim. One with ordinary skill would have found it obvious to apply the steps

of Wong et al. to the state machine of Lo et al. in performance of an LBIST test. Wong et al., in column 2 lines 62-67, describes an advantage of the invention as being capable of both pseudo-random and functional testing. Lo et al. column 2 lines 38-40 lists an advantage of the invention as being an improvement in test time and test coverage. And Zuraski Jr. et al., professes the advantages (column 2 lines 10-18) of a readily programmable BIST that would not need constant revision as needs change. In view of the motivations for Zuraski et al., Lo et al., and of Wong et al., one with ordinary skill in the art at the time of the invention, would combine all of the references above, thus the claim is rejected.

23. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Rosno et al., U.S. Patent No. 6535986, in view of Kraus et al., U.S. Patent No. 6587979, in view of Zuraski et al., U.S. Patent No. 6560740, in view of Lo et al., U.S. Patent No. 5661732, and Wong et al., U.S. Patent No. 6636997 as applied to Claim 23, and further in view of Hong-Shin Jun, U.S. Patent No. 6658611, and of Au et al., U.S. Patent No. 6681359. The method of Claim 23 fails to further teach wherein the signature includes an error bit and a "done" bit. Jun teaches that the signature (MISR) of a test system includes an error bit (Jun column 5 lines 43-63) and a "done" bit (Au et al. column 9 lines 25-33). It would have been obvious to apply the same capabilities to the system in the subject claim to improve test pattern handling during test. Jun cites an improved programmable BIST using optimum test patterns (column 2 lines 10-13), and one with ordinary skill in the art at the time of the invention, motivated as suggested above and

as suggested previously for Au et al., would combine the references, and therefore the claim is rejected.

24. Claims 26, 31 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Au et al., U.S. Patent No. 6681359, in view of Zuraski et al., U.S. Patent No. 6560740, in view of Motika et al., U.S. Patent No. 5982189, and in view of Rosno et al., U.S. Patent No. 6535986.

As per Claim 26:

Au et al. teaches a method for testing an integrated circuit device (see Abstract), the method comprising: interfacing the integrated circuit device with a tester (column 7 lines 31-34 and column 8 lines 29-31); but fails to teach entering test via an external reset. However, in an analogous art, Zuraski et al. enters a state via an external reset signal (Zuraski et al, column 10 lines 31-36), an obvious modification in order to control the test circuit during test, but fails to teach the test being an LBIST. But Motika et al. performs a logic built-in self-test (Motika et al. column 3 lines 64-66), and obtains the results of the BIST (Motika et al. column 3 lines 55-60 and column 4 lines 1-3). It would have been obvious to apply the teachings of Motika in order to obtain test results in Au et al. However, Motika et al. fails to teach the frequency specification of the applicant. In an analogous art, Rosno et al. does teach this feature in columns 1 lines 64-67 and column 2 lines 1-12, and also column 3 lines 66-67 and column 4 lines 1-10. It would have been obvious to one with ordinary skill to add the features of Rosno et al. to Motika et al. in order to run the circuits at frequencies low enough to pass test. And in view of the motivations previously stated for the above references, the claim is rejected.

As per Claim 31:

Au et al. further teaches the method of claim 26, and obtaining the results by reading the signature (column 10 lines 21-26). And in view of the previously stated motivation, the claim is rejected.

As per Claim 32:

The method of claim 26 is further limited wherein testing interface comprises a Joint Test Action Group tap controller. Au et al., in the Abstract further teaches this feature, and cites the advantage of a controller of BIST circuits using a standard JTAG interface (column 2 lines 18-26). And in view of the previously stated motivation, the claim is rejected.

25. Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Au et al., U.S. Patent No. 6681359, in view of Zuraski et al., U.S. Patent No. 6560740, in view of Motika et al., U.S. Patent No. 5982189, and in view of Rosno et al., U.S. Patent No. 6535986 as applied to Claim 26, and further in view of Rajski et al., U.S. Patent No. 6684358. The method of Claim 26 does not teach the claim limits of resetting a MISR and a pattern generator in an LBIST. But Rajski et al. performs these functions on an LBIST (column 4 lines 10-57). And it would have been obvious to apply this reset to the control circuits prior to start-up of the subject test thereby guaranteeing a starting basis. In column 2 lines 15-33, Rajski et al. recites an improved pattern generator that allows fuller test coverage than predecessors. One with ordinary skill in the art at the time of the invention, motivated as suggested by Rajski et al., would combine the references, and so the claim is rejected.

26. Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Au et al., U.S. Patent No. 6681359, in view of Zuraski et al., U.S. Patent No. 6560740, in view of Motika et al., U.S. Patent No. 5982189, and in view of Rosno et al., U.S. Patent No. 6535986 as applied to Claim 26 above, and further in view of Lo et al., U.S. Patent No. 5661732, and Wong et al., U.S. Patent No. 6636997. The method of Claim 26 fails to teach an initialize, scan, and step method as claimed in the subject claim. In an analogous art, Lo et al., enters a 1st state subsequent to a start ABIST signal (Lo et al. column 5 lines 6-8), and suggests a similar LBIST on the same chip (column 6 lines 9-12). In order to control operation of the test cycles, it would have been obvious to provide the features of Lo et al. in the same circuit under consideration. And finally, Wong et al. in column 6 lines 26-50 teaches the states of scan, step, and complete (done) as specified by the applicant's claim. One with ordinary skill would have found it obvious to apply the steps of Wong et al. to the state machine of Lo et al. in performance of an LBIST test. Wong et al., in column 2 lines 62-67, describes an advantage of the invention as being capable of both pseudo-random and functional testing. Lo et al. column 2 lines 38-40 lists an advantage of the invention as being an improvement in test time and test coverage. In view of the motivations for Lo et al., and in view of Wong et al., one with ordinary skill in the art at the time of the invention, would combine all of the references above, thus the claim is rejected.

27. Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Au et al., U.S. Patent No. 6681359, in view of Zuraski et al., U.S. Patent No. 6560740, in view of Motika et al., U.S. Patent No. 5982189, in view of Rosno et al., U.S. Patent No.

6535986, in view of Lo et al., U.S. Patent No. 5661732, and Wong et al., U.S. Patent No. 6636997 as applied to Claim 28 above, and further in view of Hong-Shin Jun, U.S. Patent No. 6658611. The method of Claim 28 fails to teach the limitation wherein the signature includes an error bit and a "done" bit. Jun teaches that the signature (MISR) includes an error bit (Jun column 5 lines 43-63) and a "done" bit (Au et al. column 9 lines 25-33). It would have been obvious to apply the teachings therefrom in order to facilitate control of test states. Jun also cites an improved programmable BIST using optimum test patterns (column 2 lines 10-13), and one with ordinary skill in the art at the time of the invention, motivated as suggested above and as suggested previously for Au et al., would combine the references, and therefore the claim is rejected.

28. Claim 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over Au et al., U.S. Patent No. 6681359, in view of Zuraski et al., U.S. Patent No. 6560740, in view of Motika et al., U.S. Patent No. 5982189, and in view of Rosno et al., U.S. Patent No. 6535986 as applied to Claim 26 above, in view of Kraus et al., U.S. Patent No. 6587979. Rosno et al. further teaches a method for performing a BIST (see Abstract) on an IC device, but not specified is that the controller be reset externally. However, in an analogous art, the BIST of Kraus et al., resets the BIST controller of FIG.7 by way of the tester 21 (column 9 lines 52-58), and performs an MBIST (column 15 lines 24-35), and obtains results (column 8 lines 10-36) of the BIST. It would have been obvious to provide a means of resetting the circuit under test as taught by Kraus et al. in order to improve test flexibility. And column 2 lines 32-40 of Kraus et al. explains the attributes of the invention as being a highly adaptable and flexible platform for testing, and one with

ordinary skill in the art at the time of the invention, motivated by Kraus et al., would combine the references, as so the claim is rejected.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John P Trimmings whose telephone number is 703-305-0714. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on 703-305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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